HCSL/LVCMOS Clock Generator

IDT6T49278BI

DATA SHEET

General Description

The IDT6T49278BI is a PLL-based clock generator for Freescale systems. This high performance device is optimized to generate the processor core reference clock, the PCI-Express, sRIO, XAUI, SerDes reference clocks and the clocks for both the Gigabit Ethernet MAC and PHY. The clock generator offers ultra low-jitter, low-skew clock outputs. The output frequencies are generated from a 25MHz external input source or an external 25MHz parallel resonant crystal. The industrial temperature range of the IDT6T49278BI supports telecommunication, networking, and storage requirements.

Applications

- CPE Gateway Design
- Home Media Servers
- 802.11n AP or Gateway
- Soho Secure Gateway
- Soho SME Gateway
- Wireless Soho and SME VPN Solutions
- Wired and Wireless Network Security
- Web Servers and Exchange Servers

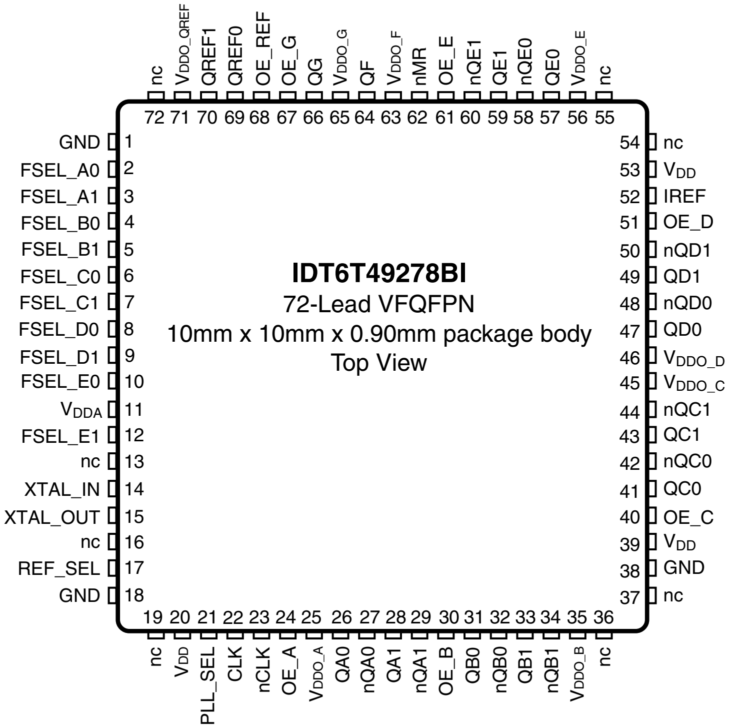
Features

- Ten selectable 100MHz, 125MHz, 156.25MHz and 312.5MHz clocks for PCI Express, sRIO and GbE, HCSL interface levels
- One single-ended QG LVCMOS/LVTTL clock output at 125MHz
- One single-ended QF LVCMOS/LVTTL clock output at 50MHz, 15Ω output impedance
- Two single-ended QREFx LVCMOS/LVTTL outputs at 25MHz, 15Ω output impedance
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential CLK, nCLK input pair that can accept: LVPECL, LVDS, LVHSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Supply Modes, (125MHz QG output and 25MHz QREFx outputs):

  Core / Output
  3.3V / 3.3V
  3.3V / 2.5V
- Supply Modes, (HCSL outputs, and 50MHz QF output):

  Core / Output
  3.3V / 3.3V
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) package

Pin Assignment



Block Diagram

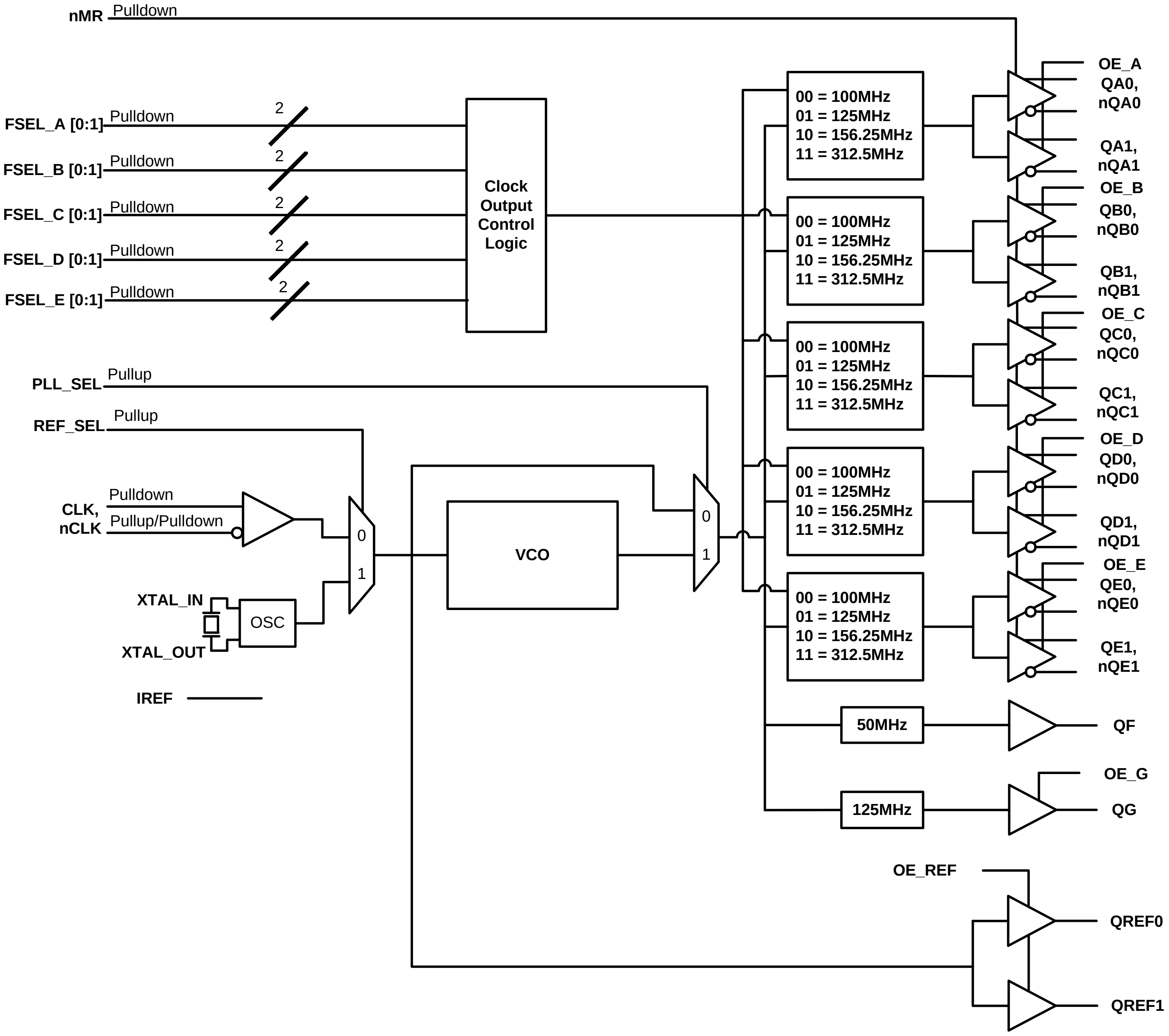


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 18, 38	GND	Power		Power supply ground.
2, 3	FSEL_A0. FSEL_A1	Input	Pulldown	Selects the QAx, nQAx output frequency. See Table 3A. LVCMOS/LVTTL interface levels.
4, 5	FSEL_B0, FSEL_B1	Input	Pulldown	Selects the QBx, nQBx output frequency. See Table 3A. LVCMOS/LVTTL interface levels.
6, 7	FSEL_C0, FSEL_C1	Input	Pulldown	Selects the QCx, nQCx output frequency. See Table 3A. LVCMOS/LVTTL interface levels.
8, 9	FSEL_D0, FSEL_D1	Input	Pulldown	Selects the QDx, nQDx output frequency. See Table 3A. LVCMOS/LVTTL interface levels.
10, 12	FSEL_E0, FSEL_E1	Input	Pulldown	Selects the QEx, nQEx output frequency. See Table 3A. LVCMOS/LVTTL interface levels.
11	V_{DDA}	Power		Analog supply pin.
13, 16, 19, 36, 37, 54, 55, 72	nc	Unused		No connect.
14, 15	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
17	REF_SEL	Input	Pullup	Input source control pin. See Table 3C. LVCMOS/LVTTL interface levels.
20, 39, 53	V_{DD}	Power		Core supply pins.
21	PLL_SEL	Input	Pullup	PLL bypass control pin. See Table 3B. LVCMOS/LVTTL interface levels.
22	CLK	Input	Pulldown	Non-inverting differential clock input.
23	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
24	OE_A	Input	Pullup	Active HIGH output enable for Bank A outputs. See Table 3D. LVCMOS/LVTTL interface levels.
25	V_{DDO_A}	Power		Bank A (HCSL) output supply pin. 3.3 V supply.
26, 27	QA0, nQA0	Output		Differential output pairs. HCSL interface levels.
28, 29	QA1, nQA1	Output		Differential output pairs. HCSL interface levels.
30	OE_B	Input	Pullup	Active HIGH output enable for Bank B outputs. See Table 3D. LVCMOS/LVTTL interface levels.
31, 32	QB0, nQB0	Output		Differential output pair. HCSL interface levels.
33, 34	QB1, nQB1	Output		Differential output pair. HCSL interface levels.
35	V_{DDO_B}	Power		Bank B (HCSL) output supply pin. 3.3V supply.
40	OE_C	Input	Pullup	Active HIGH output enable for Bank C outputs. See Table 3D. LVCMOS/LVTTL interface levels.
41, 42	QC0, nQC0	Output		Differential output pair. HCSL interface levels.
43, 44	QC1, nQC1	Output		Differential output pair. HCSL interface levels.
45	V_{DDO_C}	Power		Bank C (HCSL) output supply pin. 3.3V supply.
46	V_{DDO_D}	Power		Bank D (HCSL) output and HCSL reference circuit supply pin. Must be connected to 3.3V to use any of the HCSL outputs.
47, 48	QD0, nQD0	Output		Differential output pair. HCSL interface levels.
49, 50	QD1, nQD1	Output		Differential output pair. HCSL interface levels.
Continued on next page.				

Number	Name	Type		Description
51	OE_D	Input	Pullup	Active HIGH output enable for Bank D outputs. See Table 3D. LVCMOS/LVTTL interface levels.
52	I_{REF}	Input		External fixed precision resistor (475) from this pin to ground provides a reference current used for differential current-mode Q[Ax:Ex], nQ[Ax:EX] outputs.
56	V_{DDO_E}	Power		Bank E (HCSL) output supply pin. 3.3V supply.
57, 58	QE0, nQE0	Output		Differential output pair. HCSL interface levels.
59, 60	QE1, nQE1	Output		Differential output pair. HCSL interface levels.
61	OE_E	Input	Pullup	Active HIGH output enable for Bank E outputs. See Table 3D. LVCMOS/LVTTL interface levels.
62	nMR	Input	Pulldown	Active LOW Master Reset. When logic LOW, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go low. When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
63	V_{DDO_F}	Power		QF output supply pin (LVCMOS/LVTTL). 3.3V supply.
64	QF	Output		Single-ended output. 3.3V LVCMOS/LVTTL interface levels.
65	V_{DDO_G}	Power		QG output supply pins (LVCMOS/LVTTL). 3.3V or 2.5V supply.
66	QG	Output		Single-ended output. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
67	OE_G	Input	Pullup	Active HIGH output enable for Bank G output. See Table 3E. LVCMOS/LVTTL interface levels.
68	OE_REF	Input	Pullup	Active HIGH output enable for QREF[0:1] outputs. See Table 3F. LVCMOS/LVTTL interface levels.
69, 70	QREF0, QREF1	Output		Single-ended REF outputs. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
71	V_{DDO_QREF}	Power		QREF[0:1] output supply pin (LVCMOS/LVTTL). 3.3V or 2.5V supply.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QF, QG, QREF[0:1]	$V_{DDO\_F} = V_{DDO\_G} = V_{DDO\_QREF} = 3.465V$		15		Ω
		QG, QREF[0:1]	V_{DDO_QREF}, V_{DDO_G} = 2.625V		15		Ω

Function Tables

Table 3A. FSEL_X Control Input Function Table

Input	Output Frequency
FSEL_X[0:1]	**Q[Ax:Ex], nQ[Ax:Ex]**
00 (default)	100MHz
01	125MHz
10	156.25MHz
11	312.50MHz

NOTE: FSEL_X denotes FSEL_A, _B, _C, _D, _E.
NOTE Any two outputs operated at the same frequency will be synchronous.

Table 3B. PLL_SEL Control Input Function Table

Input	
PLL_SEL	**Operation**
0	PLL Bypass
1 (default)	PLL Mode

Table 3C. REF_SEL Control Input Function Table

Input	
REF_SEL	**Clock Source**
0	CLK, nCLK
1 (default)	XTAL_IN, XTAL_OUT

Table 3D. OE_[A:E] Control Input Function Table

Input	Outputs
OE_[A:E]	**Q[Ax:Ex], nQ[Ax:Ex]**
0	High-Impedance
1 (default)	Enabled

Table 3E. OE_G Control Input Function Table

Input	Outputs
OE_G	**QG**
0	High-Impedance
1 (default)	Enabled

Table 3F. OE_REF Control Input Function Table

Input	Output
OE_REF	**QREF[0:1]**
0	High-Impedance
1 (default)	Enabled

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	25.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_[A:E]} = V_{DDO\_[F:G]} = V_{DDO\_QREF} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			86	103	mA
I_{DDA}	Analog Supply Current			13	16	mA
I_{DDO_X}	Output Supply Current	No Load, CLK selected		76	91	mA

NOTE: V_{DDO_X} denotes $V_{DDO\_[A:E]}$, $V_{DDO\_[F:G]}$, V_{DDO_QREF}.

NOTE: I_{DDO_X} denotes $I_{DDO\_[A:E]} + I_{DDO\_[F:G]} + I_{DDO\_QREF}$

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_G} = V_{DDO\_QREF} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
V_{DDO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			79	95	mA
I_{DDA}	Analog Supply Current			13	16	mA
I_{DDO_X}	Output Supply Current	No Load, CLK selected		50	60	mA

NOTE: V_{DDO_X} denotes V_{DDO_G}, V_{DDO_QREF}.

NOTE: I_{DDO_X} denotes $I_{DDO\_G} + I_{DDO\_QREF}$.

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_F} = 3.3V \pm 5\%$; or $V_{DD} = 3.3V \pm 5\%$, $V_{DDO\_G} = V_{DDO\_QREF} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nMR, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_D[0:1], FSEL_E[0:1]	$V_{DD} = V_{IN} = 3.465V$			150	µA
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	$V_{DD} = V_{IN} = 3.465V$			10	uA
I_{IL}	Input Low Current	nMR, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_D[0:1], FSEL_E[0:1]	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			uA
V_{OH}	Output High Voltage		$V_{DDO\_F} = V_{DDO\_G}$, $V_{DDO\_QREF} = 3.465V$, $I_{OH} = -12mA$	2.6			V
			V_{DDO_G}, $V_{DDO\_QREF} = 2.625V$, $I_{OH} = -12mA$	1.8			V
V_{OL}	Output Low Voltage		$V_{DDO\_F} = V_{DDO\_G}$, $V_{DDO\_QREF} = 3.465V$ or V_{DDO_G}, $V_{DDO\_QREF} = 2.625V$, $I_{OH} = 12mA$			0.6	V

Table 4D. Differential DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nCLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		$V_{DD} - 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

Table 6. Input Frequency Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; or V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK, nCLK			25		MHz
		XTAL_IN, XTAL_OUT			25		MHz

AC Electrical Characteristics

Table 7A. PCI Express Jitter Specifications, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		14.27	24.35	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	ƒ = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		1.47	3.04	3.10	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	ƒ = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.17	0.67	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	ƒ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.37	0.79	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 7B. Serial Rapid IO Switch Jitter Specification, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	IDT sRIO Specification	Units
J_{CLK_REF}	Total Phase Jitter, RMS; NOTE 1, 2, 3, 4	ƒ = 125MHz, 25MHz Crystal Input, HCSL Output Clocks		0.64	1.55	3	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *Serial Rapid IO Application Note section* in the datasheet.
NOTE 1: Total phase jitter after applying the evaluation bands to the system transfer function for the IDT sRIO Tsi57x and Tsi620 Product Families. The transfer function is defined and illustrated in the *Serial Rapid IO Application Note section* in the datasheet and the IDT hardware manual of the Tsi57x and Tsi620. Total RMS phase jitter allowed on the reference clock of the Tsi57x and Tsi620 is specified at 3ps (max).
NOTE 2: Evaluation band with sRIO mask applied: 10Hz - 40MHz.
NOTE 3: Total phase jitter includes random and deterministic jitter.
NOTE 4: Jitter data is measured with Agilent E5052A Signal Source Analyzer.

Table 7C. Jitter Specifications for Network Processor Core Clocks and High Speed PLLs, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Output	Minimum	Typical	Maximum	Units
J_{CORE_REFCLK}	Total Jitter; Peak-to-Peak NOTE 1, 2, 3	*f* = 50MHz, 25MHz Crystal Input, Internal Processor PLL BW=1MHz	QF		32.8	70	ps
		f = 50MHz, 25MHz Crystal Input, Internal Processor PLL BW=2MHz	QF		33	70.01	ps
		f = 50MHz, 25MHz Crystal Input, Internal Processor PLL BW = 5MHz	QF		33.6	70.05	ps
		f = 50MHz, 25MHz Crystal Input, Internal Processor PLL BW = 8MHz	QF		34.5	71.2	ps
		f = 50MHz, 25MHz Crystal Input, Internal Processor PLL BW = 10MHz	QF		35.3	71.9	ps
J_{PLL_REFCLK}	Total Jitter, Peak-to-Peak NOTE 1, 2, 3	*f* = 125MHz, 25MHz Crystal Input, High Speed PLL BW = 1MHz	QG		39.5	86.7	ps
		f = 125MHz, 25MHz Crystal Input, High Speed PLL BW = 2MHz	QG		39.5	86.7	ps
		f = 125MHz, 25MHz Crystal Input, High Speed PLL BW = 5MHz	QG		39.9	86.9	ps
		f = 125MHz, 25MHz Crystal Input, High Speed PLL BW = 8MHz	QG		41.6	88.4	ps
		f = 125MHz, 25MHz Crystal Input, High Speed PLL BW = 10MHz	QG		43.3	90	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *Network Processor Core Clocks and High Speed PLLs Application Note section* in the datasheet.
NOTE 1: Total phase jitter after applying the evaluation bands to the system transfer function for Network Processor Clock Architecture and High Speed PLLs. The transfer function is defined and illustrated in the *Network Processor Core Clocks and High Speed PLLs Application Note section* in the datasheet.
NOTE 2: Measurement in the Frequency Domain. Evaluation Band with PLL mask applied: 10Hz - 40MHz.
NOTE 3: Jitter data is measured with Agilent E5052A Signal Source Analyzer.

Table 7D. AC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Output	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FSEL_[A:E] = 00	Q[A:E], nQ[A:E]		100		MHz
		FSEL_[A:E] = 01	Q[A:E], nQ[A:E]		125		MHz
		FSEL_[A:E] = 10	Q[A:E], nQ[A:E]		156.25		MHz
		FSEL_[A:E] = 11	Q[A:E], nQ[A:E]		312.5		MHz
			QF		50		MHz
			QG		125		MHz
			QREF[0:1]		25		MHz

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 7E. HCSL AC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Output Configurations	Outputs	Minimum	Typical	Maximum	Units
R_J	Random Jitter	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = Disabled	QA, nQA		3	4	ps
			QB, nQB		3	4	ps
			QC, nQC		3	5	ps
			QD, nQD		3	5	ps
			QE, nQE		3	5	ps
D_J	Deterministic Jitter	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = Disabled	QA, nQA		26	55	ps
			QB, nQB		43	90	ps
			QC, nQC		48	80	ps
			QD, nQD		32	60	ps
			QE, nQE		60	85	ps
tjit(Ø)	RMS Phase Jitter, (Random) Integration Range: (12kHz to 20MHz)	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = Disabled	QA, nQA		0.77	0.96	ps
			QB, nQB		0.75	0.94	ps
			QC, nQC		0.75	1.00	ps
			QD, nQD		0.78	0.96	ps
			QE, nQE		0.76	0.95	ps
			QF		0.94	1.09	ps
			QG		0.88	1.13	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Refer to Applications Section for peak-to-peak jitter calculations.

Table 7F. HCSL AC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Output Configurations	Outputs	Minimum	Typical	Maximum	Units
R_J	Random Jitter	QA = QB = 100MHz, QC = QD = QE = 156.25MHz, QF = 50MHz, QG = 125MHz, QREF0 = QREF1 = Disabled	QA, nQA		3	4	ps
			QB, nQB		3	4	ps
			QC, nQC		3	5	ps
			QD, nQD		3	6	ps
			QE, nQE		3	5	ps
D_J	Deterministic Jitter	QA = QB = 100MHz, QC = QD = QE = 156.25MHz, QF = 50MHz, QG = 125MHz, QREF0 = QREF1 = Disabled	QA, nQA		33	65	ps
			QB, nQB		27	60	ps
			QC, nQC		62	100	ps
			QD, nQD		61	110	ps
			QE, nQE		62	100	ps
tjit(Ø)	RMS Phase Jitter, (Random) Integration Range: (12kHz to 20MHz)	QA = QB = 100MHz, QC = QD = QE = 156.25MHz, QF = 50MHz, QG = 125MHz, QREF0 = QREF1 = Disabled	QA, nQA		0.67	0.80	ps
			QB, nQB		0.68	0.82	ps
			QC, nQC		0.70	0.92	ps
			QD, nQD		0.75	0.89	ps
			QE, nQE		0.76	0.91	ps
			QF		0.93	1.07	ps
			QG		0.88	1.01	ps

For NOTES, see Table 7E above.

Table 7G. HCSL AC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Output Configurations	Outputs	Minimum	Typical	Maximum	Units
R_J	Random Jitter	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = 25MHz	QA, nQA		3	5	ps
			QB, nQB		3	5	ps
			QC, nQC		3	5	ps
			QD, nQD		3	5	ps
			QE, nQE		3	5	ps
D_J	Deterministic Jitter	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = 25MHz	QA, nQA		20	50	ps
			QB, nQB		43	100	ps
			QC, nQC		64	100	ps
			QD, nQD		30	80	ps
			QE, nQE		70	120	ps
tjit(Ø)	RMS Phase Jitter, (Random) Integration Range: (10kHz to 1.5MHz)	QA = QD = 100MHz, QB = QG = 125MHz, QC = QE = 156.25MHz, QF = 50MHz, QREF0 = QREF1 = 25MHz	QA, nQA; QD, nQD		0.66	0.76	ps
	RMS Phase Jitter, (Random) Integration Range: (1.5MHz to 50MHz)		QA, nQA; QD, nQD		0.56	0.68	ps
	RMS Phase Jitter, (Random) Integration Range: (20MHz to 78.125MHz)		QC, nQC; QE, nQE		0.34	0.48	ps
	RMS Phase Jitter, (Random) Integration Range: (12kHz to 50MHz)		QC, nQC; QE, nQE		0.85	0.95	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Refer to Applications Section for peak-to-peak jitter calculations.

Table 7H. AC Characteristics, V_{DD} = 3.3V ± 5%, $V_{DDO\_[A:E]}$ = V_{DDO_F} = 3.3V ± 5%; and V_{DD} = 3.3V ± 5%, V_{DDO_G} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{RB}	Ring-Back Voltage Margin; NOTE 1, 2	Q[A:E], nQ[A:E]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 1, 2	Q[A:E], nQ[A:E]		500			ps
V_{MAX}	Absolute Max Output Voltage; NOTE 3, 4	Q[A:E], nQ[A:E]				1150	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 3, 5	Q[A:E], nQ[A:E]		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 3, 6, 7	Q[A:E], nQ[A:E]		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over All Edges; NOTE 3, 6, 8	Q[A:E], nQ[A:E]				140	mV
t_{SLEW+}	Rising Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]		0.6		5.5	V/ns
t_{SLEW-}	Falling Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]		0.6		5.5	V/ns
odc	Output Duty Cycle	Q[A:E], nQ[A:E]		48		52	%
tjit(Ø)	RMS Phase Jitter, (Random)	QREF[0:1]	25MHz, Integration Range: (10kHz to 5MHz)		0.6	0.96	ps
t_R / t_F	Output Rise/Fall Time	QF	20% to 80%	400		1400	ps
		QG	20% to 80%	400		1400	ps
		QREF[0:1]	20% to 80%	300		1400	ps
odc	Output Duty Cycle	QF	measured at $V_{DDO\_F}/2$	48	50	52	%
		QG	measured at $V_{DDO\_G}/2$	45	50	55	%
		QREF[0:1]	measured at $V_{DDO\_QREF}/2$	45	50	55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTES on next page.

All parameters measured at f_{OUT} unless noted otherwise.

NOTE 1: Measurement taken from differential waveform.

NOTE 2: t_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the Vrb ±100mV range. See Parameter Measurement Information Section.

NOTE 3: Measurement taken from single-ended waveform.

NOTE 4: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 5: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 6: Measured at the crossing point where the instantaneous voltage value of the rising edge of Q[Ax:Ex] equals the falling edge of nQ[Ax:Ex].

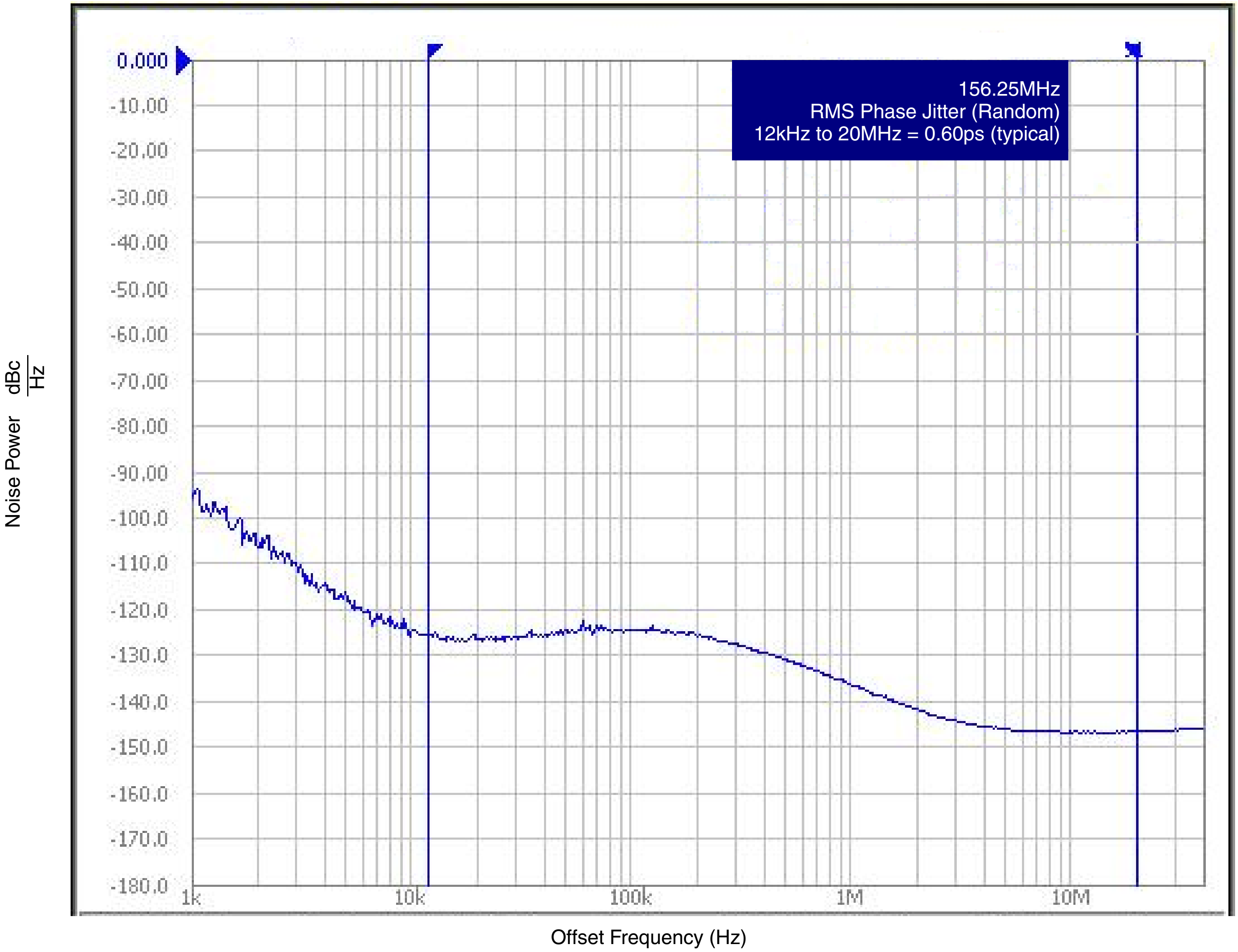
NOTE 7: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

NOTE 8: Defined as the total variation of all crossing voltages of rising Q[Ax:Ex] and falling nQ[Ax:Ex]. This is the maximum allowed variance in Vcross for any particular system.

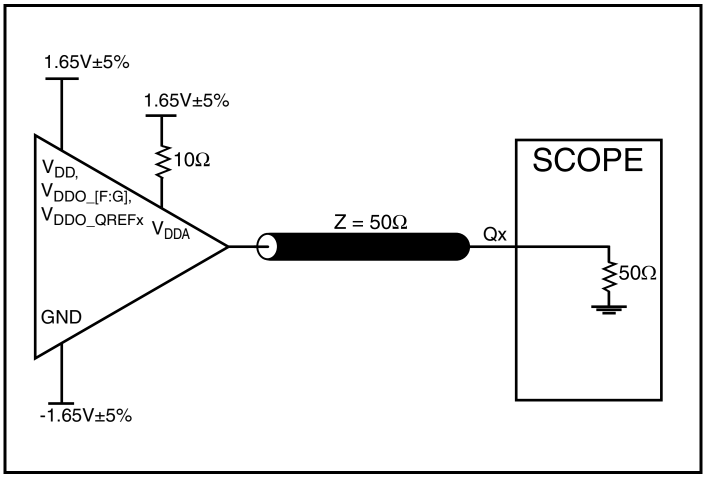
NOTES continued on next page.

NOTE 9: Measured from -150mV to +150mV on the differential waveform (derived from Q[Ax:Ex] minus nQ[Ax:Ex]). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

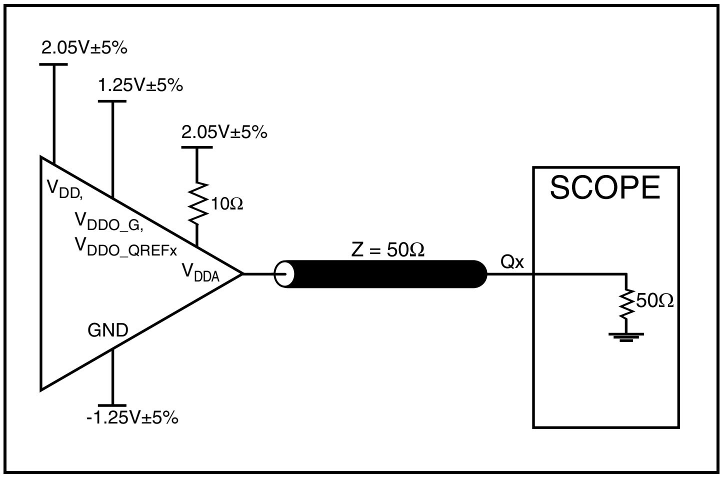
Typical Phase Noise at 156.25MHz



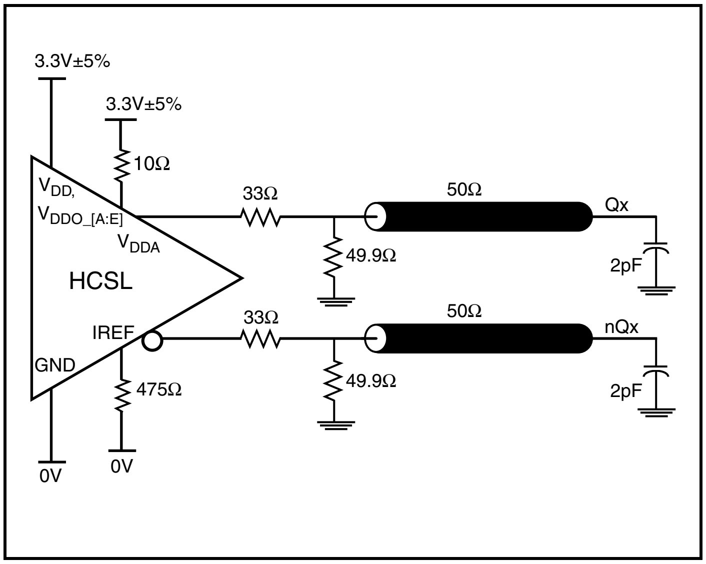
Parameter Measurement Information



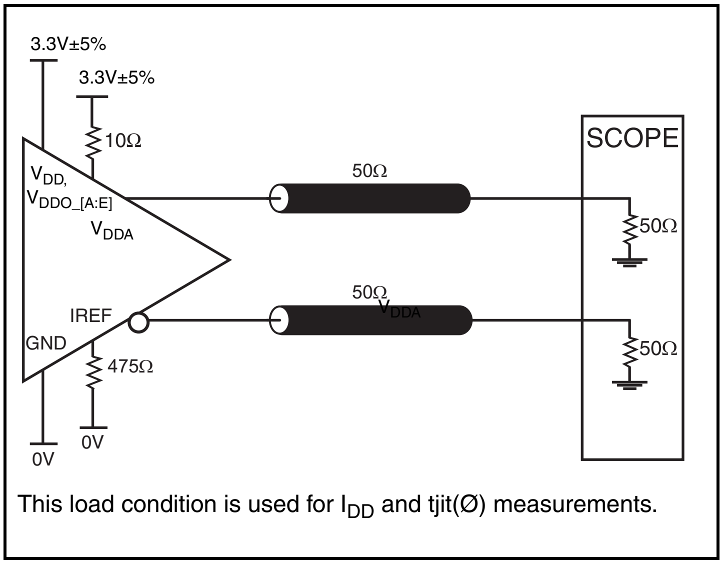
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

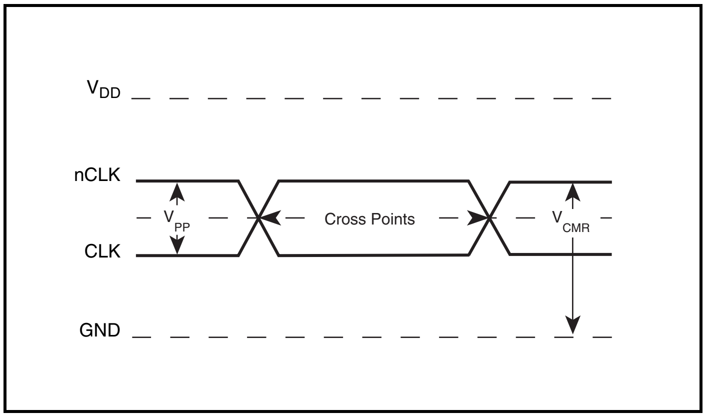


3.3V Core/3.3V HCSL Output Load AC Test Circuit

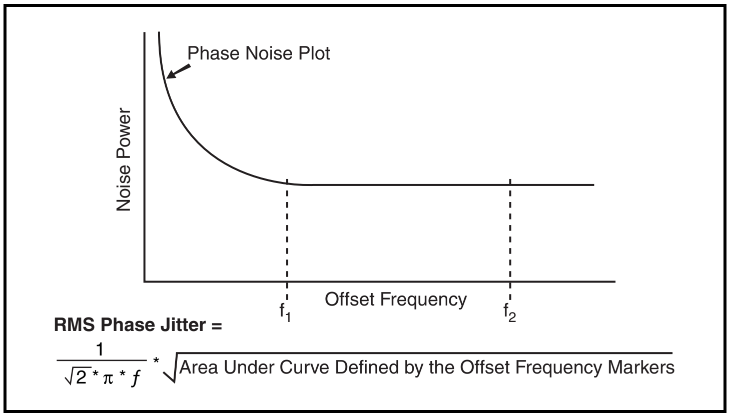


This load condition is used for I_{DD} and tjit(Ø) measurements.

3.3V Core/3.3V HCSL Output Load AC Test Circuit



Differential Input Level

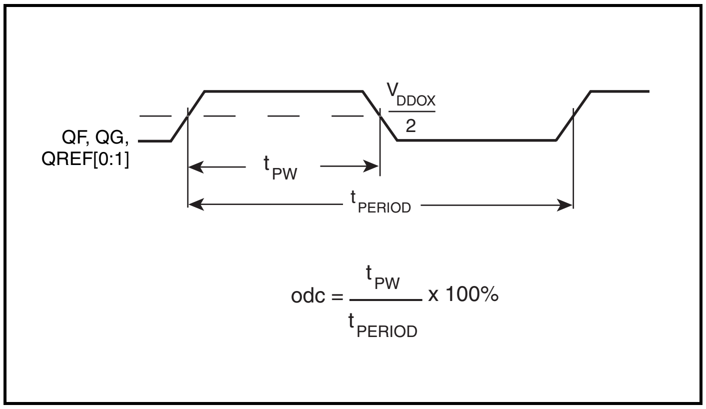


RMS Phase Jitter =

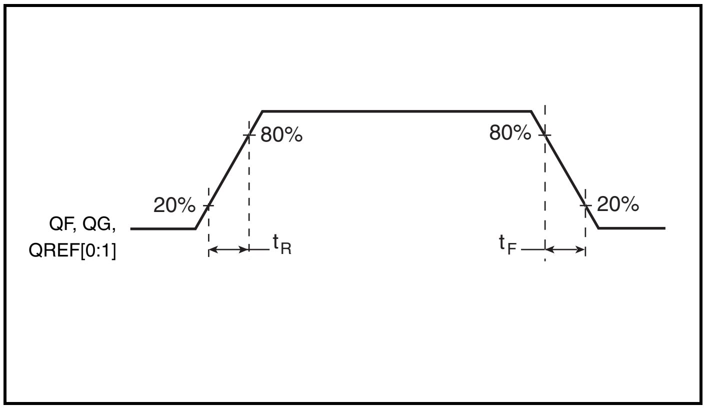
$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

RMS Phase Jitter

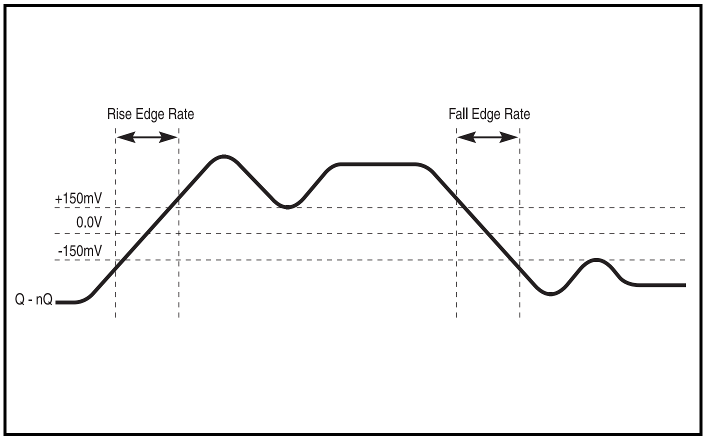
Parameter Measurement Information, continued



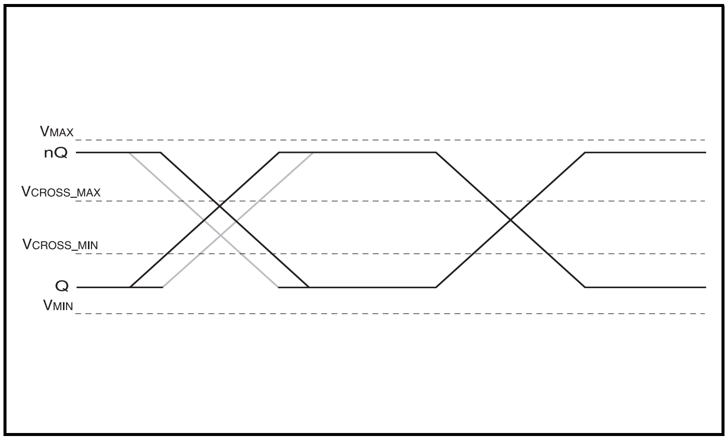
LVCMOS Output Duty Cycle/Pulse Width



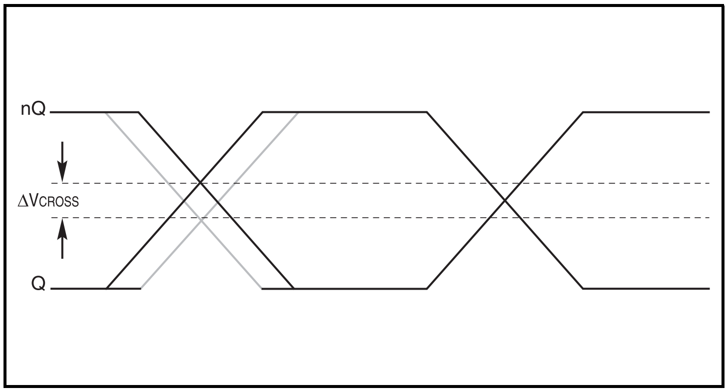
LVCMOS Output Rise/Fall Time



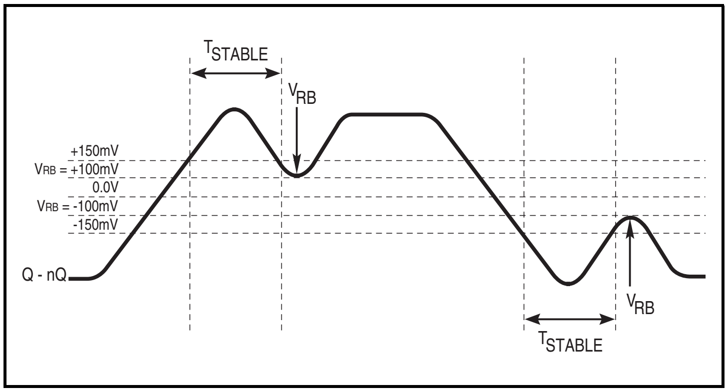
Differential Measurement Points for Rise/Fall Time Edge Rate



Single-ended Measurement Points for Absolute Cross Point/Swing

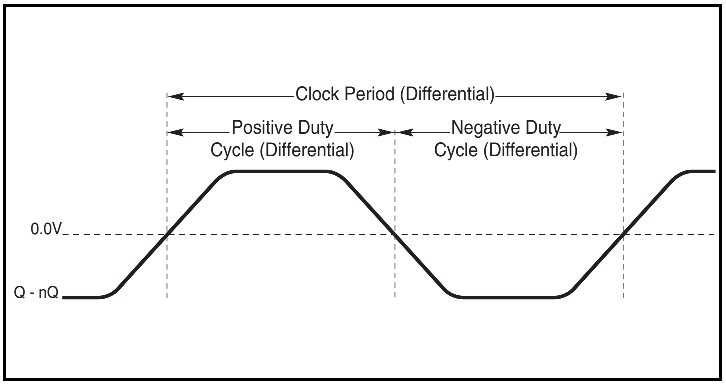


Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Ringback

Parameter Measurement Information, continued



Differential Measurement Points for Duty Cycle/Period

Peak-to-Peak Jitter Calculations

A standard deviation of a statistical population or data set is the square root of its variance. A standard deviation is used to calculate the probability of an anomaly or to predict a failure. Many times, the term "root mean square" (RMS) is used synonymously for standard deviation. This is accurate when referring to the square root of the mean squared deviation of a signal from a given baseline and when the data set contains a Gaussian distribution with no deterministic components. A low standard deviation indicates that the data set is close to the mean with little variation. A large standard deviation indicates that the data set is spread out and has a large variation from the mean.

A standard deviation is required when calculating peak-to-peak jitter. Since true peak-to-peak jitter is random and unbounded, it is important to always associate a bit error ratio (BER) when specifying a peak-to-peak jitter limit. Without it, the specification does not have a boundary and will continue get larger with sample size. Given that a BER is application specific, many frequency timing devices specify jitter as an RMS. This allows the peak-to-peak jitter to be calculated for the specific application and BER requirement. Because a standard deviation is the variation from the *mean* of the data set, it is important to always calculate the peak-to-peak jitter using the typical RMS value.

The *Table 8* shows the BER with its appropriate RMS Multiplier. There are two columns for the RMS multiplier, one should be used if your signal is data and the other should be used if the signal is a repetitive clock signal. The difference between the two is the data transition density (DTD). The DTD is the number of rising or falling transitions divided by the total number of bits. For a clock signal, they are equal, hence the DTD is 1. For Data, on average, most common encoding standards have a 0.5 DTD.

Table 8. BER Table

BER	RMS Multiplier Data, "DTD = 0.5"	RMS Multiplier Clock, "DTD = 1"
10^{-3}	6.180	6.582
10^{-4}	7.438	7.782
10^{-5}	8.530	8.834
10^{-6}	9.507	9.784
10^{-7}	10.399	10.654
10^{-8}	11.224	11.462
10^{-9}	11.996	12.218
10^{-10}	12.723	12.934
10^{-11}	13.412	13.614
10^{-12}	14.069	14.260
10^{-13}	14.698	14.882
10^{-14}	15.301	15.478
10^{-15}	15.883	16.028

Once the BER is chosen, there are two circumstances to consider. Is the data set purely Gaussian or does it contains any deterministic component? If it is Gaussian, then the peak to peak jitter can be calculated by simply multiplying the RMS multiplier with the typical RMS specification. For example, if a 10^{-12} BER is required for a clock signal, multiply 14.260 times the typical jitter specification.

Jitter (peak-to-peak) = RMS Multiplier * RMS (typical)

If the datasheet contains deterministic components, then the random jitter (R_J) and deterministic jitter (D_J) must be separated and analyzed separately. $R_{J,}$ also known as Gaussian jitter, is not bounded and the peak-to-peak will continue to get larger as the sample size increases. Alternatively, peak-to-peak value of D_J is bounded and can easily be observed and predicted. Therefore, the peak to peak jitter for the random component must be added to the deterministic component. This is called total jitter (T_J).

Total Jitter (peak-to-peak) = [RMS Multiplier * Random Jitter (R_J)] + Deterministic Jitter (D_J)

The *total jitter equation* is not specific to one type of jitter classification. It can be used to calculate BER on various types of RMS jitter. It is important that the user understands their jitter requirement to ensure they are calculating the correct BER for their jitter requirement.

NOTE: Use R_J and D_J values for AC Characteristics Tables 7B through 7G to calculate T_J.

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

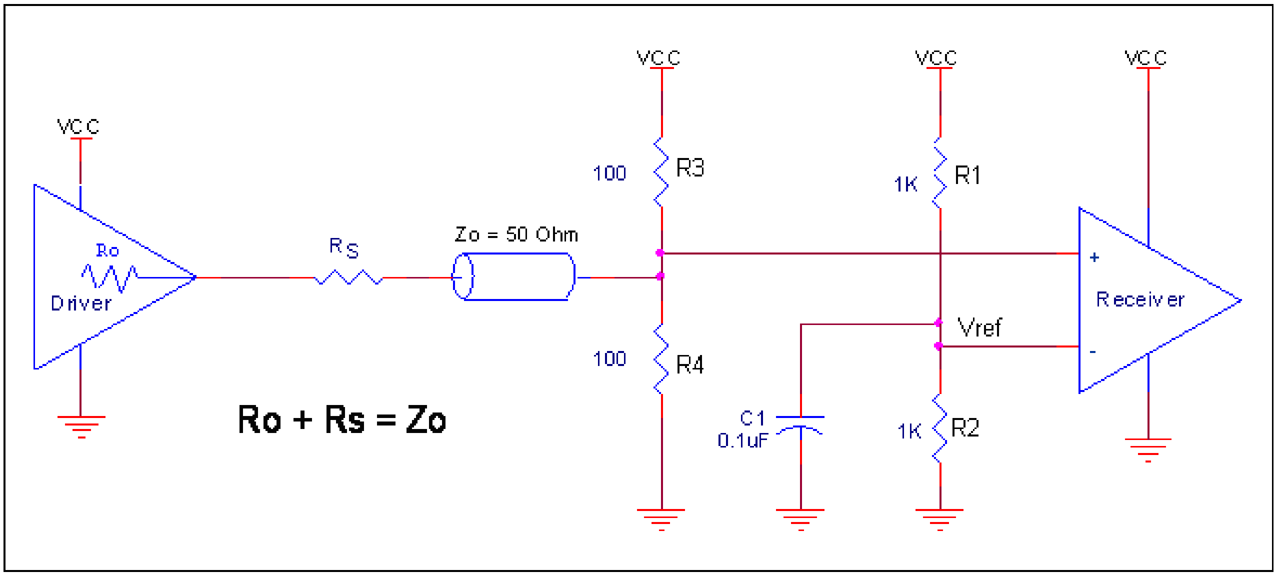


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

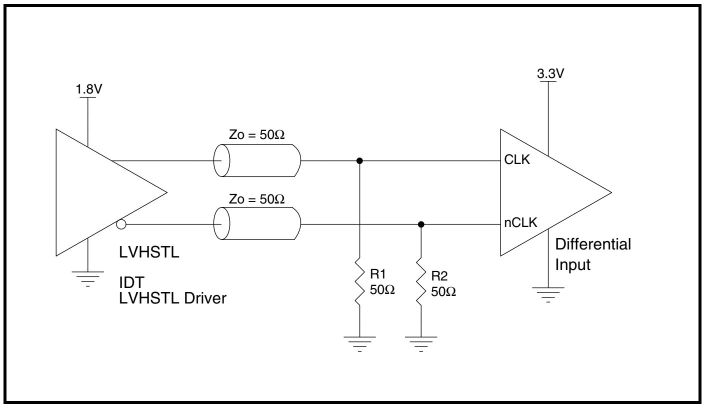


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

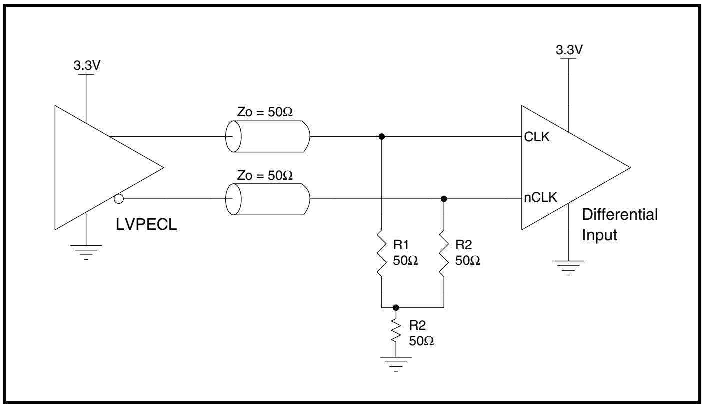


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

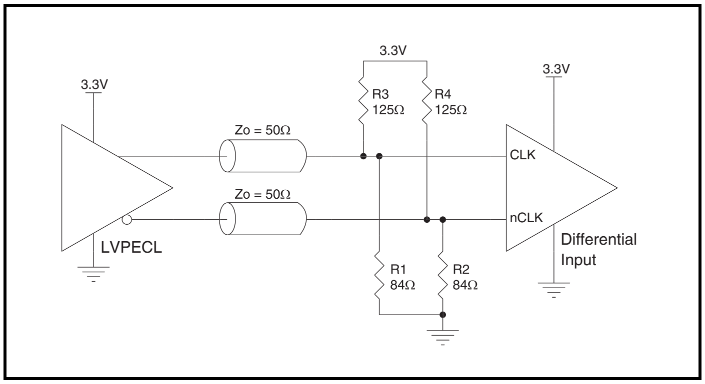


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

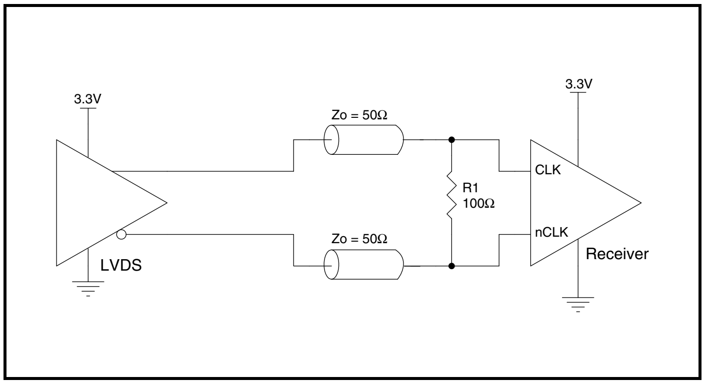


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

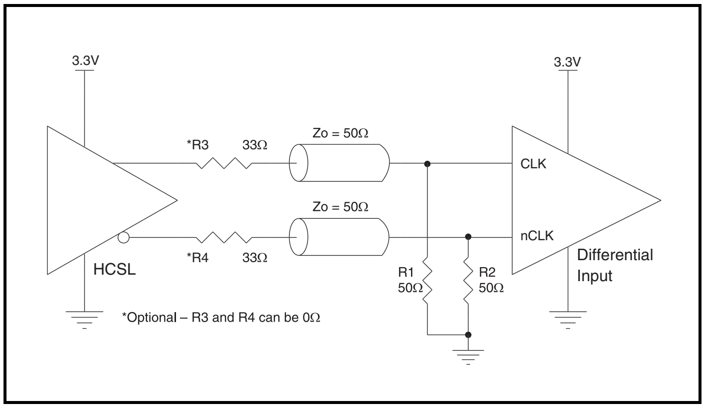


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

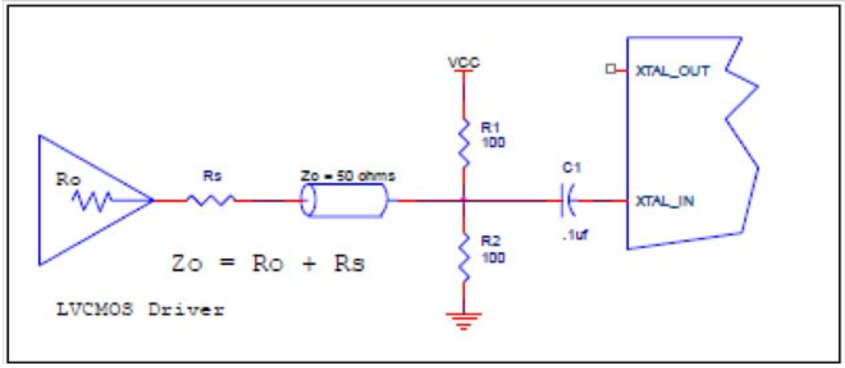


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

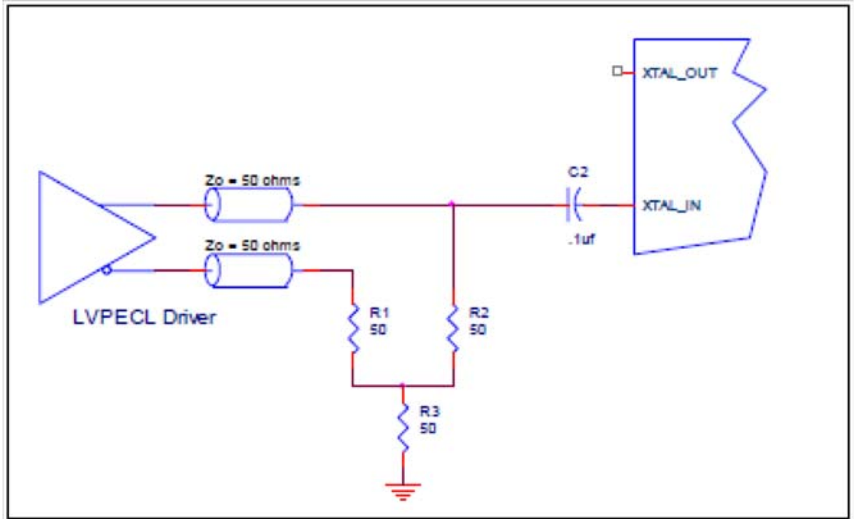


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

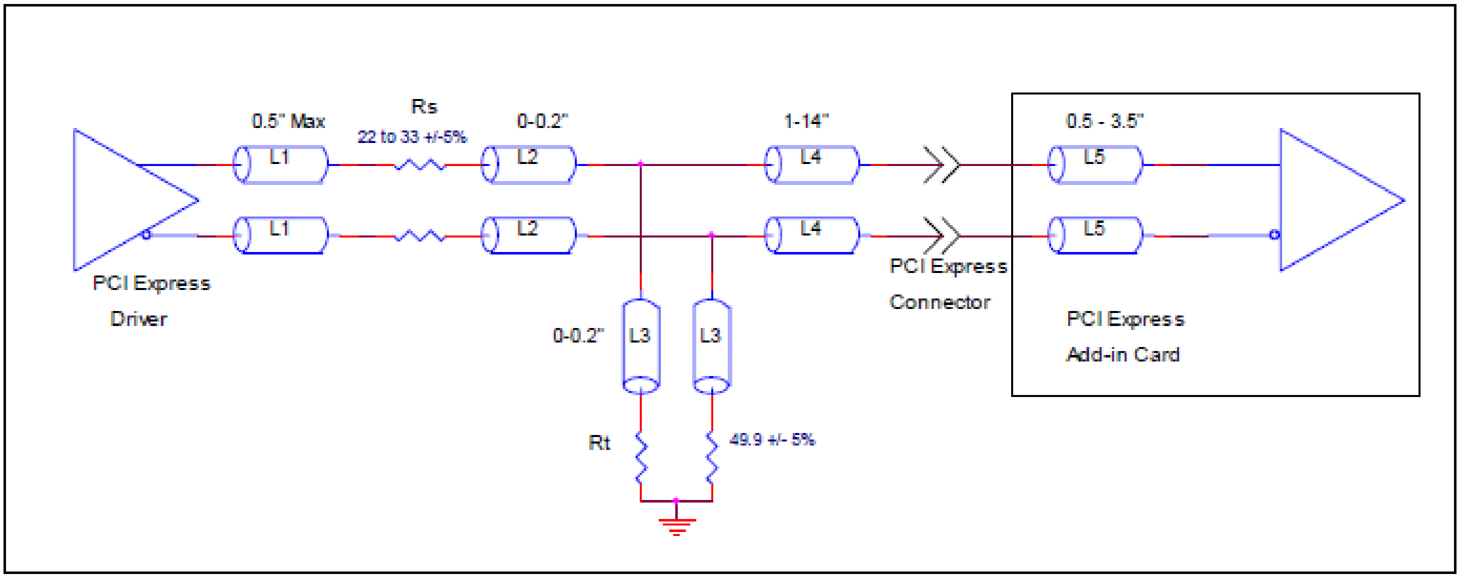


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

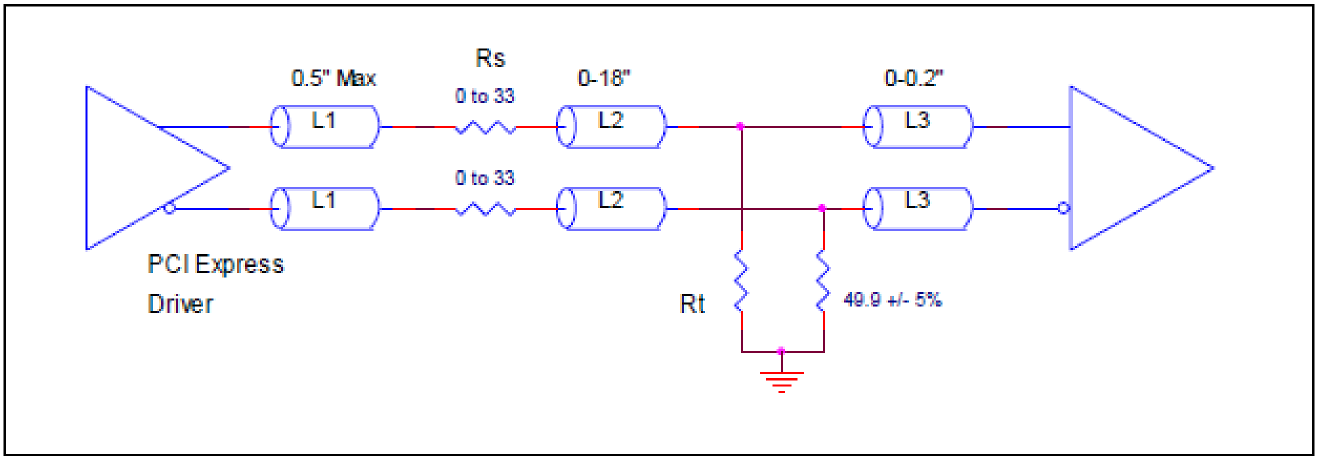


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

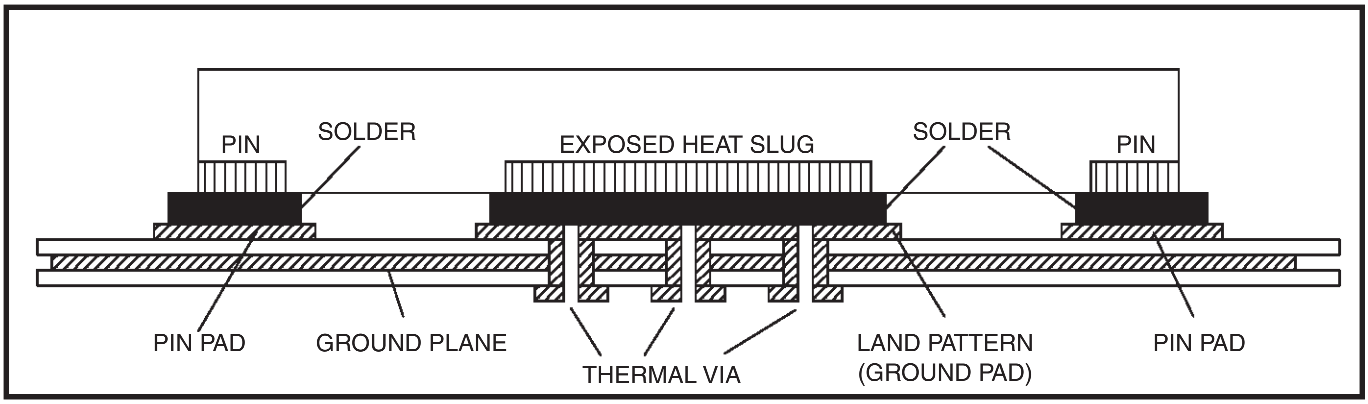


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Schematic Example

Figure 6 (next page) shows an example of IDT6T49278BI application schematic. In this example, the device is operated at $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = V_{DDO\_C} = V_{DDO\_D} = V_{DDO\_E} = V_{DDO\_F} = V_{DDO\_QREF} =$ 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 22pF and C2 = 10pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT6T49278BI provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

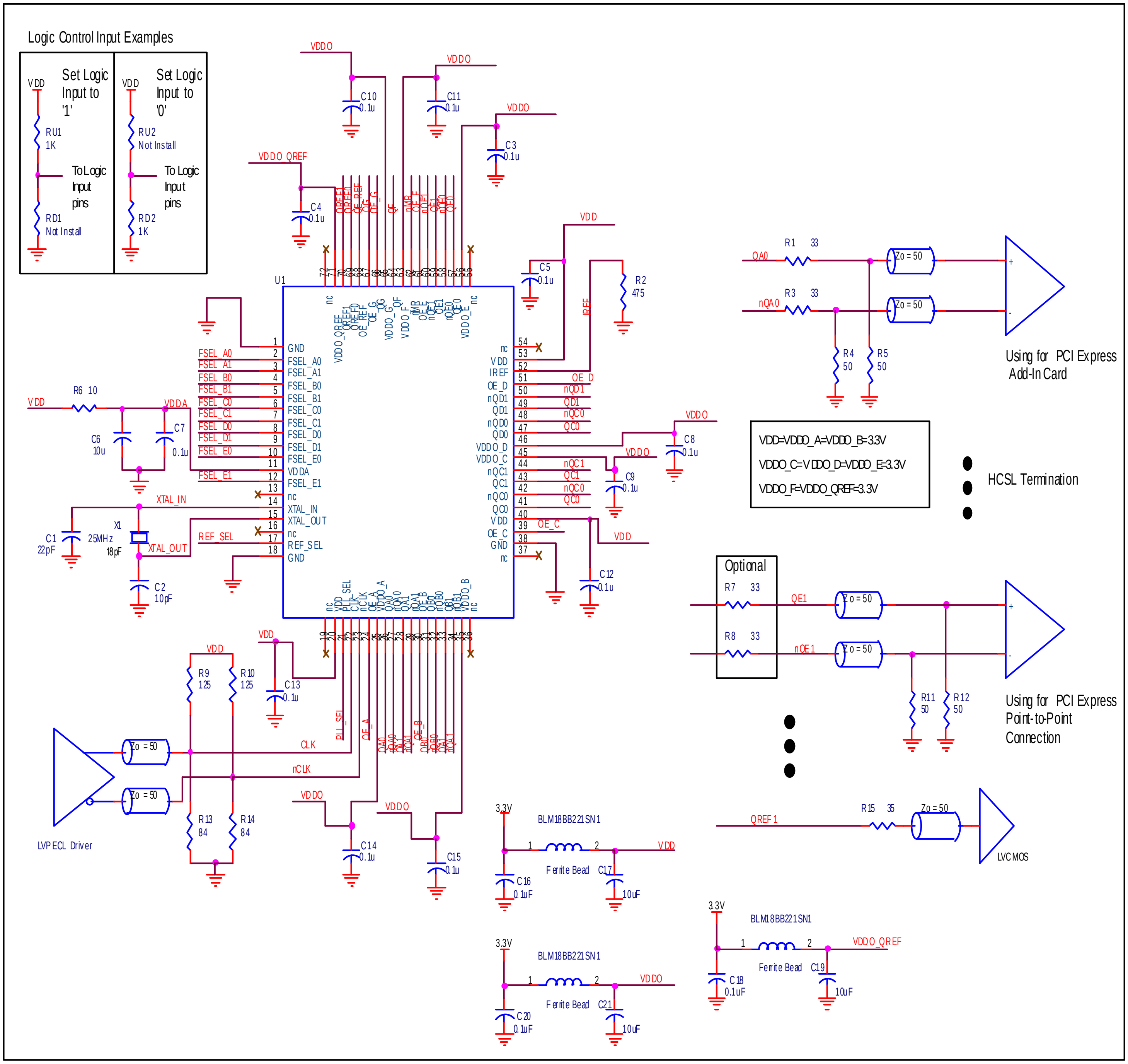


Figure 6. IDT6T49278BI Schematic Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

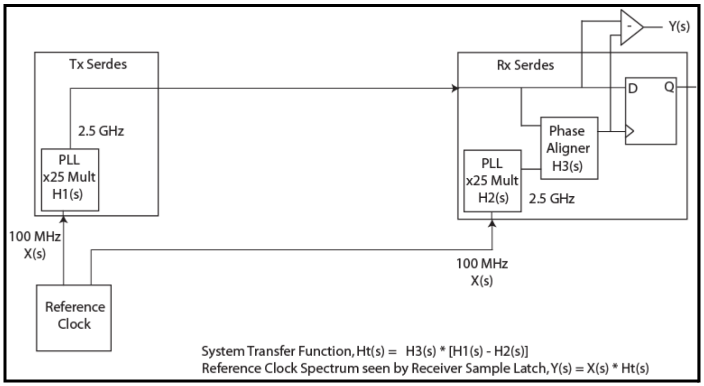
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

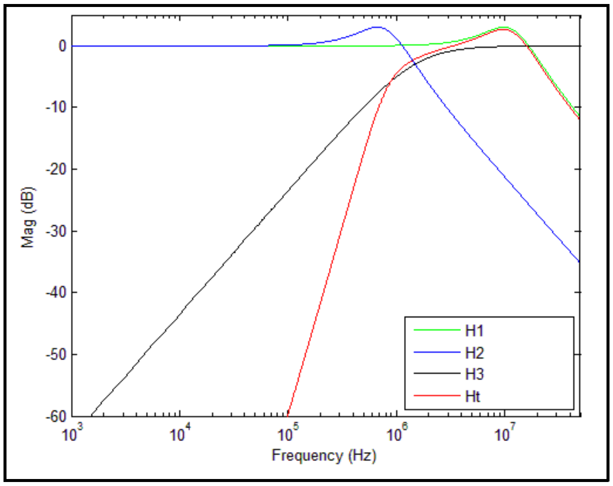
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



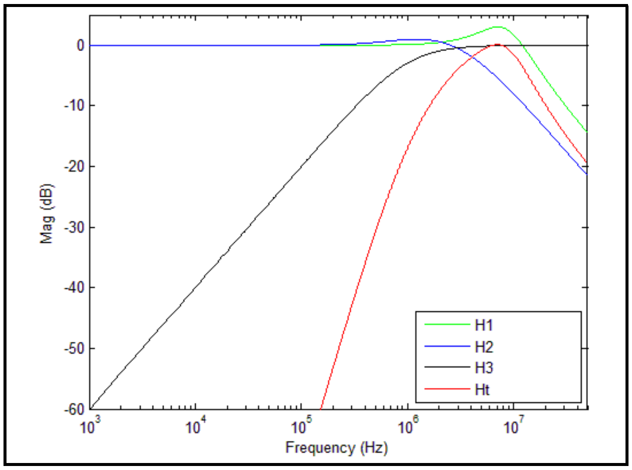
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

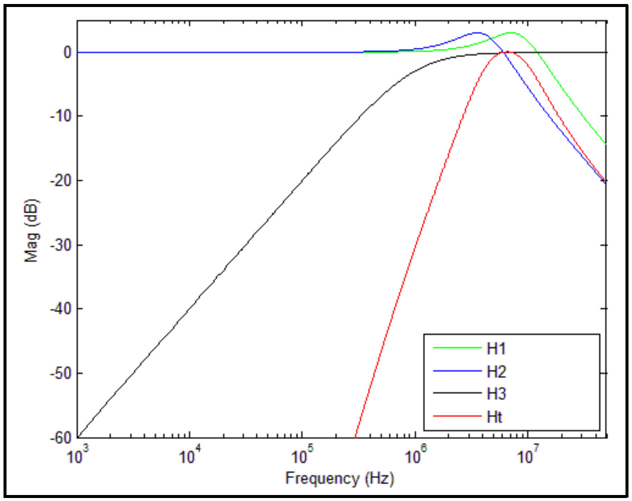


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

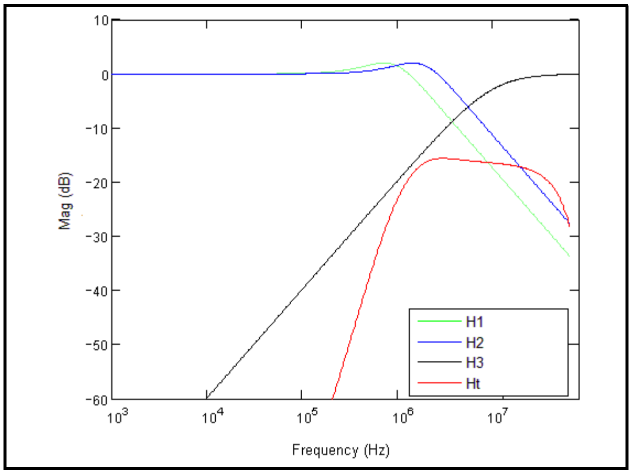


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Serial Rapid IO Application Note

The Serial Rapid IO jitter analysis methodology models the system response to reference clock jitter. The total RMS phase jitter allowed on the reference clock of the Tsi57x and Tsi620 is specified at 3ps (max). In this jitter analysis, the TSI57x and Tsi620 SERDES PLL is modeled by the transfer response function H(s) shown in *Figure 7.* To model the response of the switch on the reference clock jitter, a phase noise measurement is executed and a frequency domain analysis is performed. In the phase noise plot, the mask of the transfer function H(s) is applied to the phase noise response of the reference clock. The area under the resultant phase noise curve is referred to as Phase Jitter. In the frequency domain, the random and deterministic jitter can be calculated quickly and accurately. RMS Phase Jitter is also referred to as random jitter and the spurs on the phase noise plot can be interpreted as deterministic jitter. Total RMS Phase Jitter includes both random and deterministic jitter.

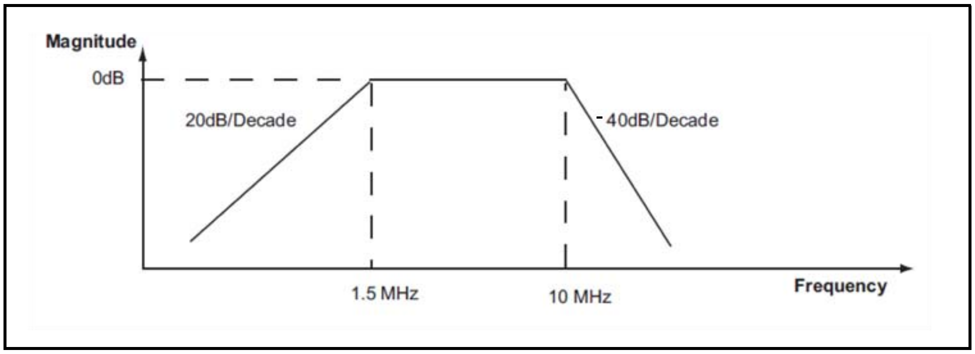


Figure 7. Weighing Function for Jitter Calculation

Network Processor Core Clocks and High Speed PLLs Application Note

The Network Processor Core clocks and High Speed PLLs jitter analysis models the system response to reference clock jitter. Network Processors typically have internal high speed PLLs that scale external reference core clocks 10x, 20x and 40x the input frequency. In this jitter analysis, the high speed PLLs internal to the processors are modeled by the transfer response function shown in *Figure 8.* A phase noise measurement is executed and a frequency domain analysis is performed. In the phase noise plot, the high speed PLL transfer function is masked on the reference clock. The area under the resultant phase noise curve is referred to as Phase Jitter. In the frequency domain, the random and deterministic jitter can be calculated quickly and accurately. RMS Phase Jitter is also referred to as random jitter and the spurs on the phase noise plot can be interpreted as deterministic jitter. Total Phase Jitter includes both Random and Deterministic jitter. The Total Jitter can then be calulated using a desired bit error rate (BER). For additional information on calculating Total Jitter refer to the *Peak-to-Peak Jitter Calculations section*.

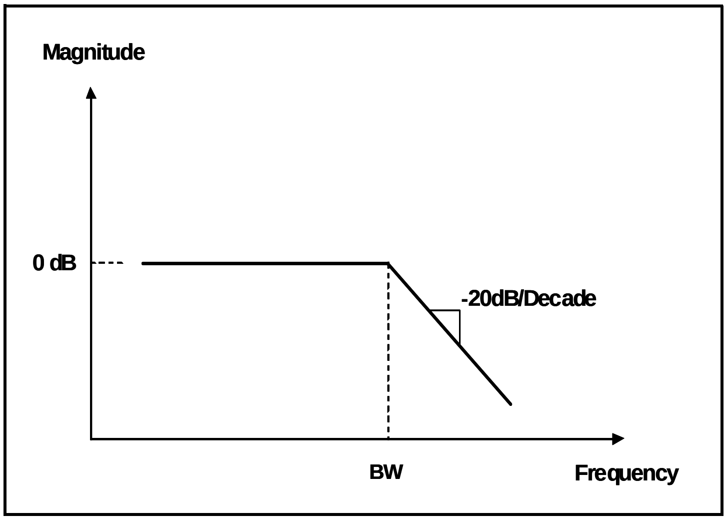


Figure 8. Weighing Function for Jitter Calculation

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT6T49278BI. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT6T49278BI is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDA})= 3.465V * (103mA + 16mA) = **412.3mW**
- Power (HCSL)$_{MAX}$ = (3.465V – 17mA * 50) 17mA = **44.5mW** per output
- Total Power (HCSL)$_{MAX}$ = 44.5mW * 10 = **445mW**

LVCMOS Driver Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DD}/2
  Output Current I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **27mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (LVCMOS) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(27mA)^2$ = **11mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 11mW * 4 = **44mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Total Power (HCSL) + Total Power (R_{OUT})
  = 412.3mW + 445mW + 44mW
  = 901.3mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.4°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.901W * 25.4°C/W = 108°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for 72 Lead VFQFPN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	25.4°C/W	20.5°C/W	18.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 9.*

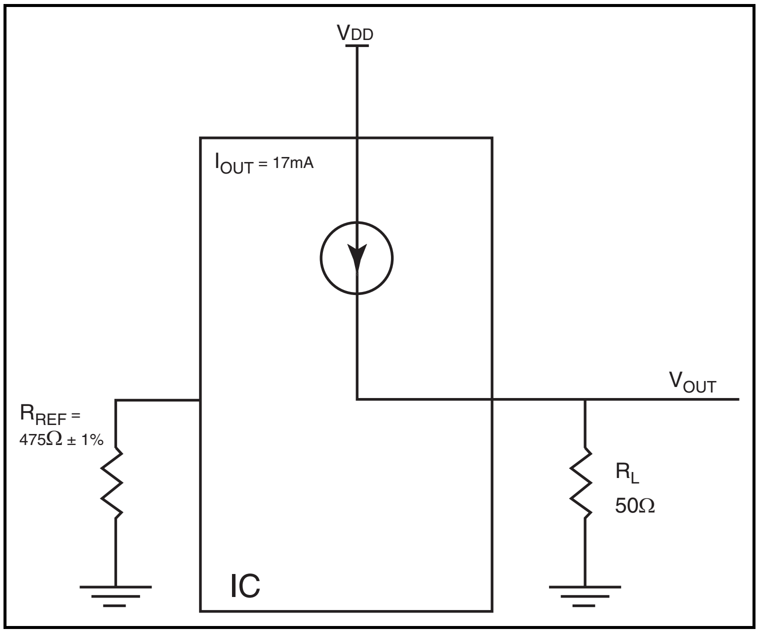


Figure 9. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD-MAX}.

Power = $(V_{DD\_MAX} – V_{OUT}) * I_{OUT}$
since $V_{OUT} = I_{OUT} * R_L$

Power = $(V_{DD\_MAX} – I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 10. θ_{JA} vs. Air Flow Table for a 72 Lead VFQFPN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	25.4°C/W	20.5°C/W	18.4°C/W

Transistor Count

The transistor count for IDT6T49278BI is: 10,297

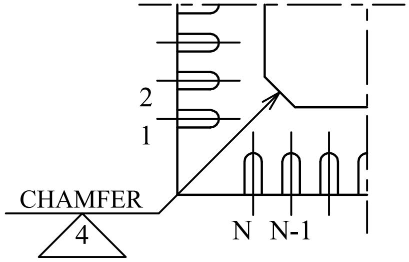
Package Outline and Package Dimensions

Table 11. Package Dimensions - 72 Lead VFQFPN

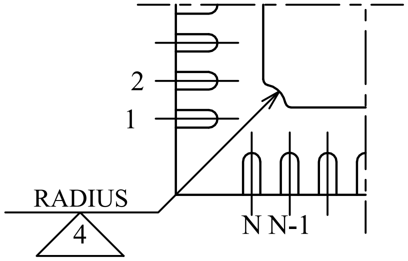
All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N	72		
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0.58	0.65	1.00
A3	0.20 Ref.		
b	0.18	0.25	0.30
N_D & N_E			18
D & E	10.00 Basic		
D1 & E1	9.75 Basic		
D2 & E2	5.50	6.00	6.60
e	0.50 Basic		
θ	8°	10°	12°
L	0.30	0.40	0.50
R (ref)	b min/2		
R1		0.20	
T	0.45 Ref.		
aaa			0.15
bbb			0.10
ccc			0.10
ddd			0.05
Θ	0		14

Reference Document: PSC-4111

Bottom View w/Type A ID



Bottom View w/Type C ID

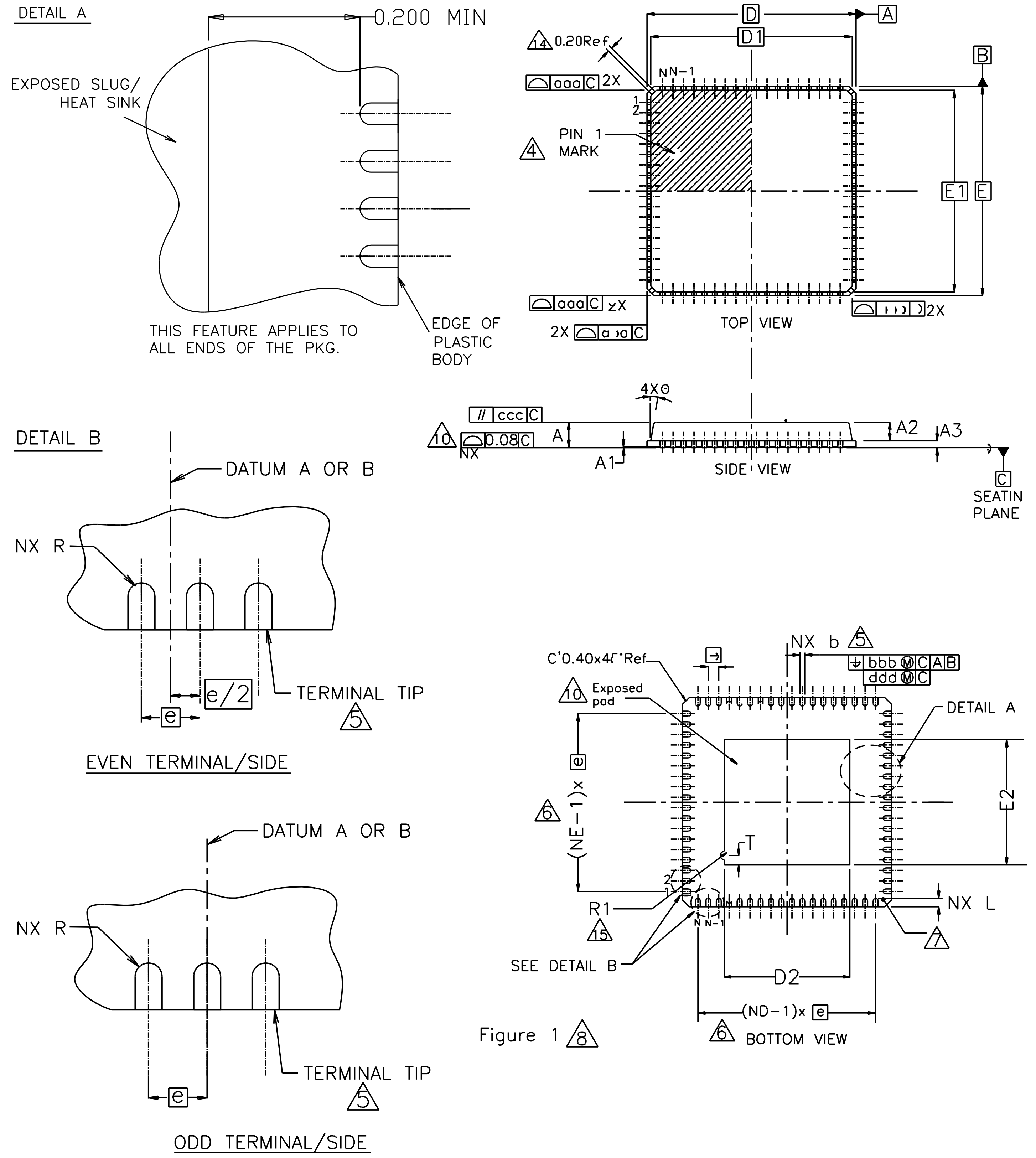


There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Package Outline

Package Outline - 72 Lead VFQFPN



Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
6T49278BNLGI	IDT6T49278BNLGI	Lead-Free, 72 Lead VFQFPN	Tray	-40°C to 85°C
6T49278BNLGI8	IDT6T49278BNLGI	Lead-Free, 72 Lead VFQFPN	500 Tape & Reel	-40°C to 85°C

NOTE: “G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			Initial release	06/19/12
A			Moved to final	04/18/13

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